IN THE SPECIFICATION:

Please replace paragraph number **[0012]** with the following rewritten paragraph:

[0012] Muraka discloses that the use of Ti as a barrier layer was found to increase the resistivity of the copper film significantly when heat-treated at temperatures of ~~350°C~~ 350° C or greater. If the heat treatment was carried out in hydrogen, no increase in resistivity was found. As this temperature is above the eutectoid temperature of a Ti-hydrogen system, the formation of TiH is assumed to have occurred. Muraka also indicates that a similar increase in resistivity is seen with Zr- and Hf-containing copper alloys. However, no data in support of this assertion is provided.

Please replace paragraph number **[0025]** with the following rewritten paragraph:

[0025] FIG. 1 shows a cross-sectional view of a semiconductor device structure 2 of the present invention. The semiconductor device structure 2 may include a semiconductor substrate 4 having a number of semiconductor devices ~~6,8~~ 6, 8. As used herein, the term "semiconductor substrate" includes a semiconductor wafer or other substrate comprising a layer of semiconductor material, such as a silicon wafer, a silicon on insulator ("SOI") substrate, a silicon on sapphire ("SOS") substrate, an epitaxial layer of silicon on a base semiconductor foundation, and other semiconductor materials such as silicon-germanium, germanium, gallium arsenide, and indium phosphide.

Please replace paragraph number **[0026]** with the following rewritten paragraph:

[0026] The semiconductor device structure 2 may optionally include a protective layer 10, which overlies the semiconductor substrate 4. The protective layer 10 prevents metal, such as copper, from contacting the semiconductor devices ~~6,8~~ 6, 8. The protective layer 10 may be formed from a silicon nitride compound, such as trisilicon tetranitride ("Si_3N_4"). The semiconductor structure 2 may also include contacts 12 that provide electrical connection to the semiconductor devices ~~6,8~~ 6, 8. These contacts 12 may include a first barrier layer (or seed

layer) 14 and a metal plug 16. The first barrier layer 14 prevents metal from the metal plug 16 from diffusing into the semiconductor devices ~~6,8~~ 6, 8.

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] The top barrier layer 28 of the semiconductor device structure may be formed on a top surface of the semiconductor device structure 2. FIGS. 2A-2E show cross-sectional views of the semiconductor device structure 2 fabricated according the present invention. FIG. 2A illustrates a portion of the semiconductor device structure 2 having a number of semiconductor devices ~~6,8~~ 6, 8. The semiconductor devices ~~6,8~~ 6, 8 may be formed in the semiconductor substrate 4 and include active semiconductor devices 6, such as transistors, and passive semiconductor devices 8, such as capacitors, or a combination of active and passive semiconductor devices ~~6,8~~ 6, 8. The semiconductor device structure 2 optionally includes the protective layer 10, which is deposited over the semiconductor substrate 4 and semiconductor devices ~~6,8~~ 6, 8. The protective layer 10 may be formed from Si_3N_4 and deposited at a thickness of about 100 nm. The dielectric layer 18 may be deposited over the protective layer 10. However, it is also contemplated that the dielectric layer 18 may be formed before the protective layer 10 and, therefore, may be present under the protective layer 10. The thickness of the dielectric layer 18 may depend on the material that is used. For instance, if the dielectric layer 18 is formed from a polymer, the polymer may be deposited to a sufficient thickness to equal a desired thickness of a first wiring level when the polymer is cured. If the dielectric layer 18 is formed from SiO_2, SiO_2 may be deposited to a thickness that is equal to the desired thickness of the first wiring level.

Please replace paragraph number **[0031]** with the following rewritten paragraph:

[0031] As shown in FIG. 2B, vias 30 may be opened to semiconductor devices ~~6,8~~ 6, 8 using photolithography techniques and etching processes. These photolithography techniques and etching processes are known in the art and may be selected for use in the present invention by a person of ordinary skill in the art. Therefore, the photolithography techniques and etching

processes are not presented here in full. The contacts 12, which include the first barrier layer 14 and the metal plug 16, may be formed in the vias 30. The first barrier layer 14 may be deposited in the vias 30 by a suitable deposition technique, such as chemical vapor deposition ("CVD"). The first barrier layer (or seed layer) 14 may be formed from a conventional material, such as titanium silicide. The metal plug 16 may be deposited in the vias 30 by a suitable deposition technique, such as CVD. The metal plug 16 may be formed from a conventional material, such as W. Excess material from the first barrier layer 14 or the metal plug 16 may be removed from the surface of the dielectric layer 18 or the protective layer 10 by chemical mechanical planarization ("CMP") or other suitable processes to form a planarized surface.

Please replace paragraph number **[0032]** with the following rewritten paragraph:

[0032] The dielectric layer 18 may be patterned to define at least one trench 32. As used herein, the term "trench" includes lines for electrically interconnecting semiconductor devices ~~6,8~~ 6, 8 in the semiconductor device structure 2. The trench 32 may be formed in the dielectric layer 18 to open up the semiconductor device structure 2 to a number of first level vias, such as vias 30. To form the trench 32, a first level metallization layer pattern may be defined in a photoresist layer formed from a conventional photoresist material. Then, the dielectric layer 18 is etched, using a conventional process, so that the first level metallization layer pattern is defined in the dielectric layer 18. The etching process may include, but is not limited to, reactive ion etching ("RIE") or an oxide etch. The photoresist layer may subsequently be removed from the semiconductor device structure 2 by a conventional process, such as a wet-strip process, a dry-strip process, or combinations thereof. This process may also remove unwanted portions of the seed layer 20 and the second barrier layer 26, such as portions that are present outside the trench 32 along a top surface of the dielectric layer 18.

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] In one embodiment of the present invention, a semiconductor device structure 2 using copper metallurgy in its entire wiring pattern is formed. A layer of about 100 nm of Si_3N_4

is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices ~~6,8~~ 6, 8 to form the protective layer 10. The dielectric layer 18, formed from polyimide, is then deposited over the protective layer 10 and cured. The polyimide layer is of sufficient thickness so that its thickness equals the first contact and wiring level of the semiconductor device structure 2 when the polyimide is cured. Contacts 12 are then opened through the polyimide layer and the protective layer. TiN is deposited to form the first barrier layer 14 and W is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the polyimide layer by CMP.

Please replace paragraph number **[0043]** with the following rewritten paragraph:

[0043] The top surfaces of the copper layer and the polyimide layer are implanted with Ti at 0.5 keV and at an implant dose of $5x10^{16}$ ions/cm^2 to form thin, metal layer 36. The Ti penetrates the copper layer an average of about 10Å and penetrates the polyimide layer about 30Å. The Ti layer is then exposed to a nitrogen plasma at ~~350°C~~ 350° C for one hour. Portions of the Ti layer overlying the copper layer react with the nitrogen to form a TiN layer while portions of the Ti layer overlying the polyimide layer form a TiC or $TiC(N)_x$ layer. This process is repeated as necessary to build a multi-level, copper polyimide wiring structure having a desired number of layers. Depending on a temperature used to apply and cure the polyimide, as well as a temperature used to deposit the photoresist layer, a final post-processing heat treatment of ~~250°C 350°C~~ 250° C-350° C for approximately 1 to 2 hours may be used to achieve the lowest resistivity conductors.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] In another embodiment, the dielectric layer 18 is formed from SiO_2. A layer of approximately 100 nm of Si_3N_4 is, optionally, deposited over the semiconductor substrate 4 and semiconductor devices ~~6,8~~ 6, 8 to form the protective layer 10. In this embodiment, the dielectric layer 18, formed from SiO_2, is formed over the Si_3N_4 layer. Contacts 12 are then opened through the SiO_2 layer and the protective layer. TiN is deposited to form the first barrier layer 14 and W

is deposited to form the metal plug 16. Excess W and TiN are subsequently removed from the surface of the protective layer 10 or the SiO_2 layer by CMP. An additional oxide layer is then applied having a thickness equal to the desired thickness of the first wiring level.

Please replace paragraph number **[0045]** with the following rewritten paragraph:

[0045] A 500Å thick layer of low temperature Si_3N_4 is then deposited, followed by a thin layer of photoresist. The desired damascene images are etched in the Si_3N_4 layer and an oxide etch is used to transfer the desired damascene images into the SiO_2 layer to define trench 32. The seed layer 20 appropriate for the electroless deposition of copper is then deposited. The photoresist layer is then removed using a selective etchant having negligible effect on the SiO_2 layer. A copper layer is selectively electrolessly deposited to form the conductor layer 22. The thickness of the copper layer is slightly less than the thickness of the SiO_2 layer. In other words, the nominal copper thickness plus the deposition tolerance equals the thickness of the SiO_2 layer. The surface of the copper layer is then implanted with Ti at 0.5 keV. The Ti penetrates the copper layer an average of about 10Å and penetrates the oxide layer about 20Å. An implant dose of $5x10^{16}$ ions per square cm is used. The Ti layer may be deposited by any other means desired. The Ti layer is exposed to a nitrogen plasma at ~~350°C~~ 350° C to form a TiN layer on the copper layer and a TiO, TiO_2, or $TiO(N)_x$ layer on the SiO_2 layer.